Who will design tomorrow's analog ICs: humans or AI-based synthesis?

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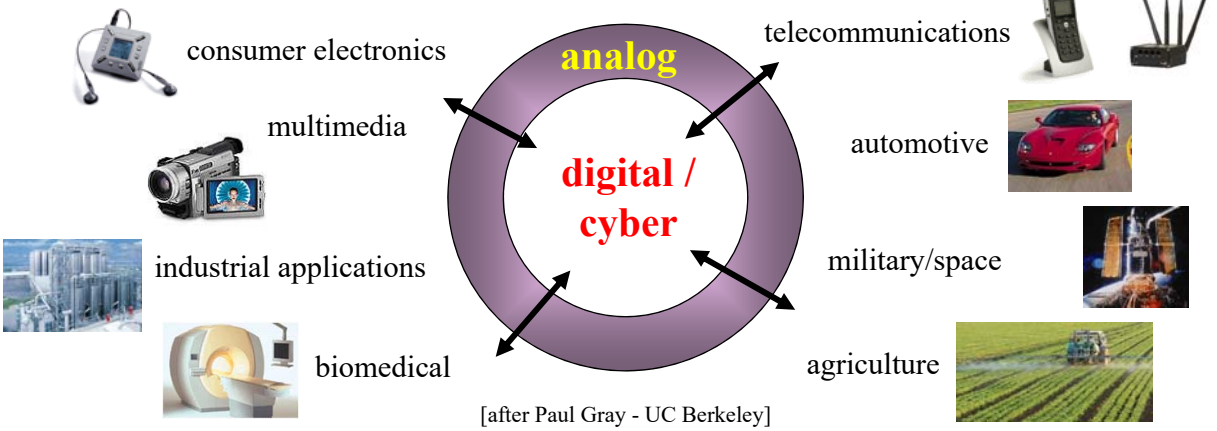
Outline

- **Analog / mixed-signal IC design**
- ML-based analog circuit sizing
- ML-based analog layout synthesis
- Conclusions

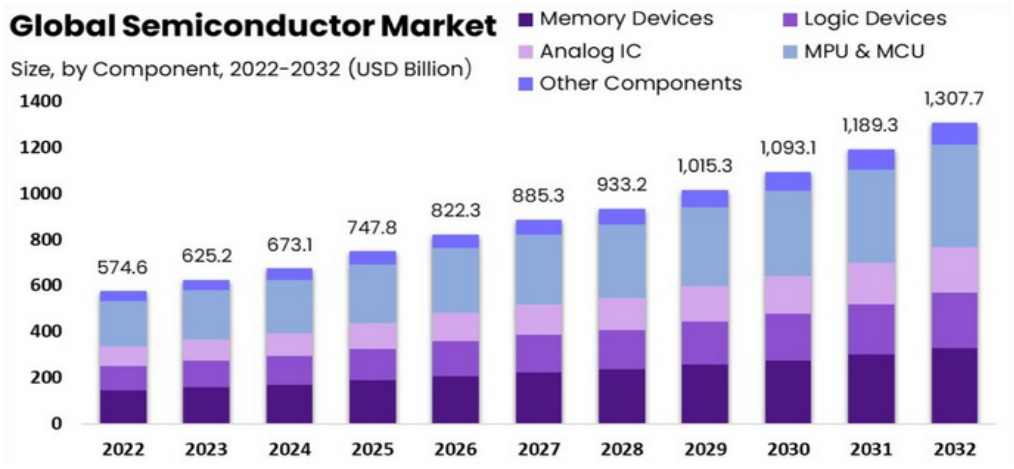
Analog in a smart digital world

- **analog / mixed-signal is the interface between the physical world and the digital cyber world**



[after Paul Gray - UC Berkeley]

Growing semiconductor business: up to 1 T$ …



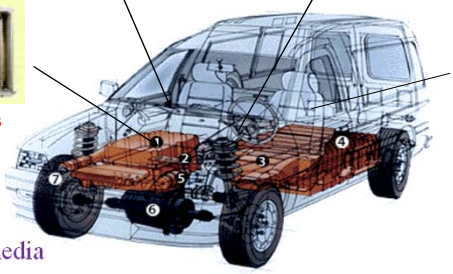
Automotive: ever better sensor interface ICs

- largest added value in new cars is provided by electronics

navigation (GPS) and telecom

passive and active security (airbag, abs, asr, active suspension)

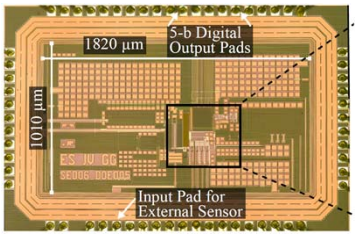
power electronics (engine control, power steering)



50 to 100 motors (windows, sunroof, airco, mirrors, seats…)

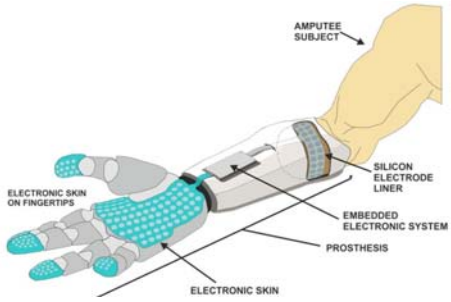
- comfort/multimedia
- active security
- assisted/autonomous driving

[Sacco JSSC 2020]



16.1 bit resolution
2nd/3rd–order noise shaping
highly-digital conversion
0.064 mm² in 0.18 mm CMOS

Biomedical: high-resolution e-skin readout

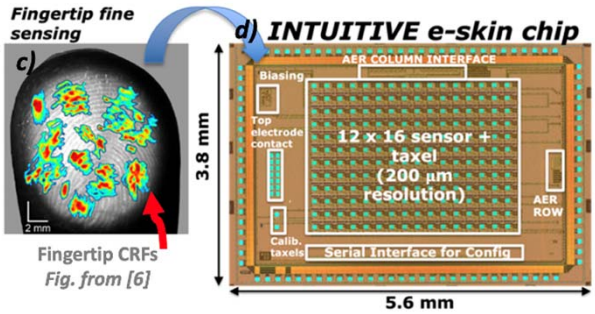


[COSMIC Lab – Univ of Genova]

- local spatial processing: ***complex receptive fields*** → texture recognition, slip detection…

Application: prosthetic/robotic hands

- **readout of tactile sensors** → asynchronous/fast spatiotemporal encoding of stimuli → "spikes"

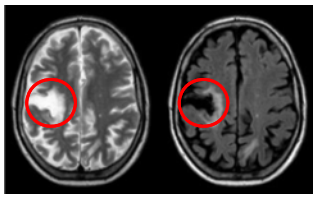


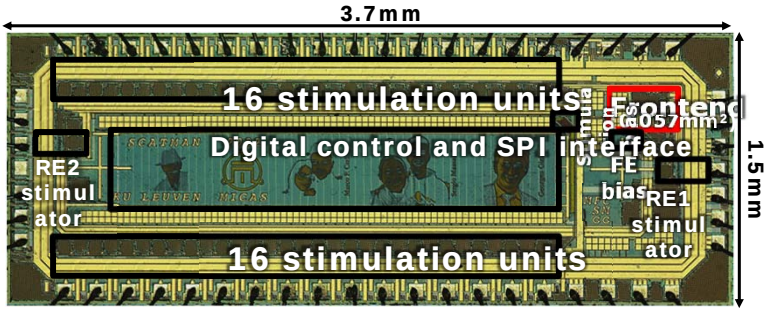
[Alea & Gielen – VLSI 2023]

Biomedical: closed-loop neural stimulation/recording

Application: closed-loop neural recording and stimulation

- **project is targeting stroke patients**

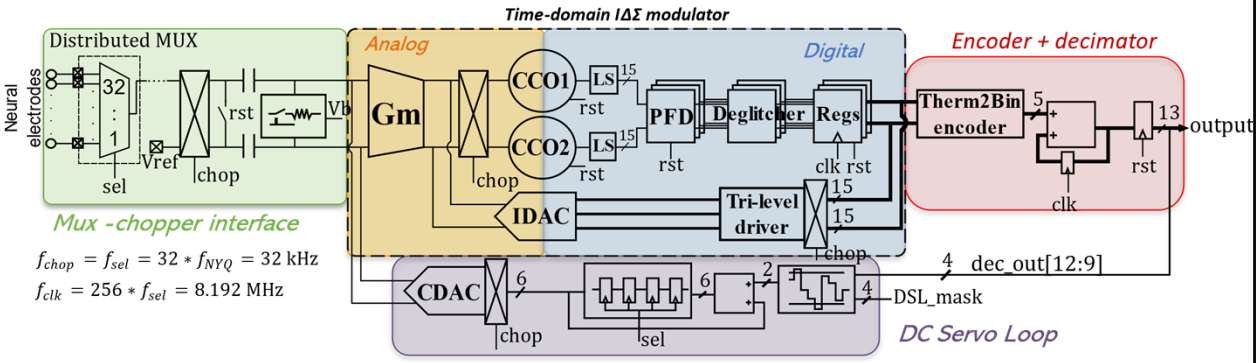




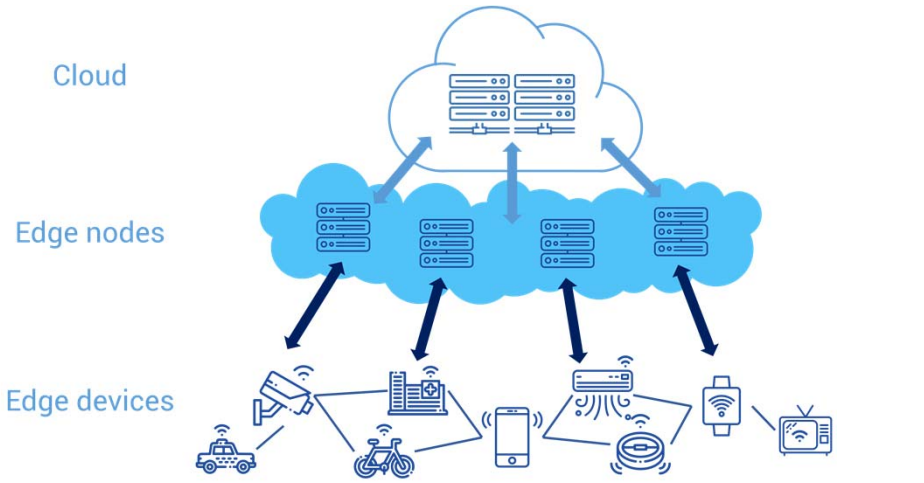
- 180 nm bulk CMOS
- 32-channel readout & stimulation
- lowest area per channel: 0.0018 mm²/ch
- low power: 4.51 µW/ch

Example biomedical: neural readout frontend

- time-based first-order incremental ΔΣ ADC
  - small area, good process scalability
  - large and variable offset cancellation



The cloud and the edge

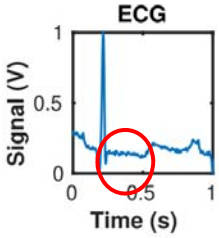


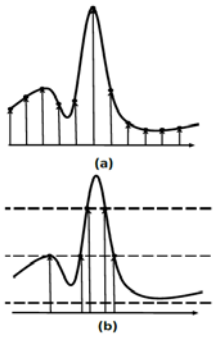
[Alibaba Cloud 2020]

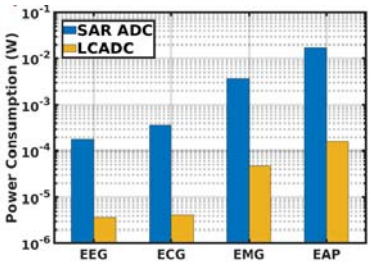
Smart (neuromorphic) processing in the edge

- mimic the brain – exploit signal properties
  - purely event-driven, self-adaptive on signal activity
  - adaptive conversion / compressive sensing

event-based sampling







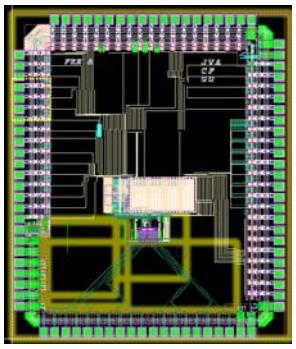
[Van Assche & Gielen
IEEE Tr. BioCAS 2020]

Neuromorphic information-driven edge computing

- efficient computing in the edge: less data, less energy, higher security, lower latency, more autonomy :

EMBODIED INTELLIGENCE

- event-driven level-crossing ADC for spiking sensor readout
- spiking neural network (SNN) for near-sensor classification
- SNN performance comparable to DNN but with lower energy/area footprint
- embedding unsupervised continual learning in the edge

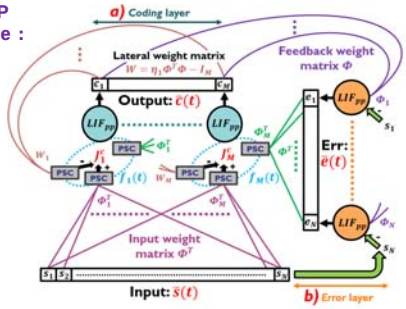


[Van Assche, Safa & Gielen Tr. BioCAS 2024]

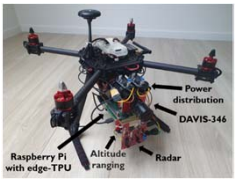
Unsupervised continual learning in the edge

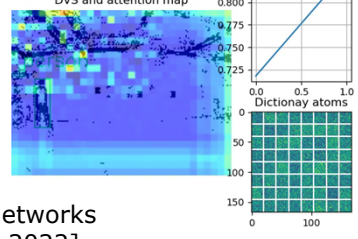
- **SNN with spike-timing-dependent plasticity (STDP)**
  - dataset collection and labeling at the edge is difficult
  - STDP step is local and works directly in the spike domain
    - compared to backprop, STDP leads to >3 orders less power
    - SNN-STDP processor can learn with $< 100\mu W$! [Frenkel Tr. BioCAS 2019]

SNN-STDP architecture :



Continual learning in action



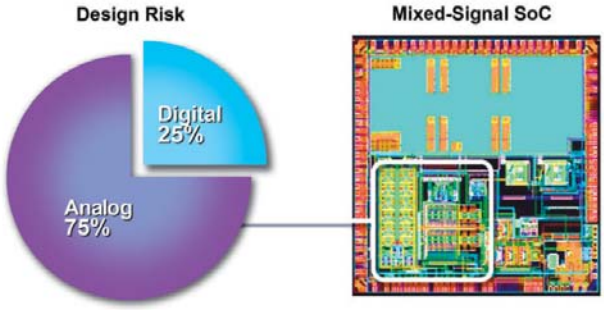


[Safa IEEE Tr. Neural Networks and Learning Systems 2022]

Low analog design productivity

- **still largely done manually**
  - long design cycles with high risk of design errors
- **high complexity in design :**
  - high-dimensional search space
  - lack of abstraction
  - unclear hierarchy
  - sensitive to all parametric effects

→ problem of **limited analog design productivity and high risk** !
  → high NRE, long time to market, several respins



[Mentor Graphics]

→ need more & better automated analog design tools

How will we design tomorrow's A/MS chips ?

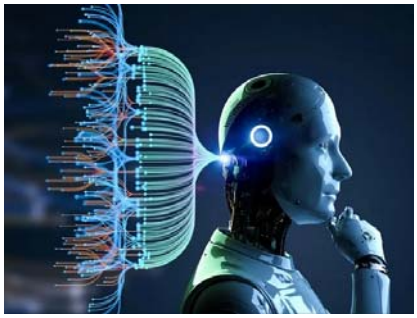
1) the heuristic-artistic way ?


[Pease Porridge]

2) today's tool-assisted / handcrafted way ?


[indiamart.com]

3) tomorrow's AI / ML-inspired synthesis / generation way ?


[studyiq.com]

Outline

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- ML-based analog layout synthesis
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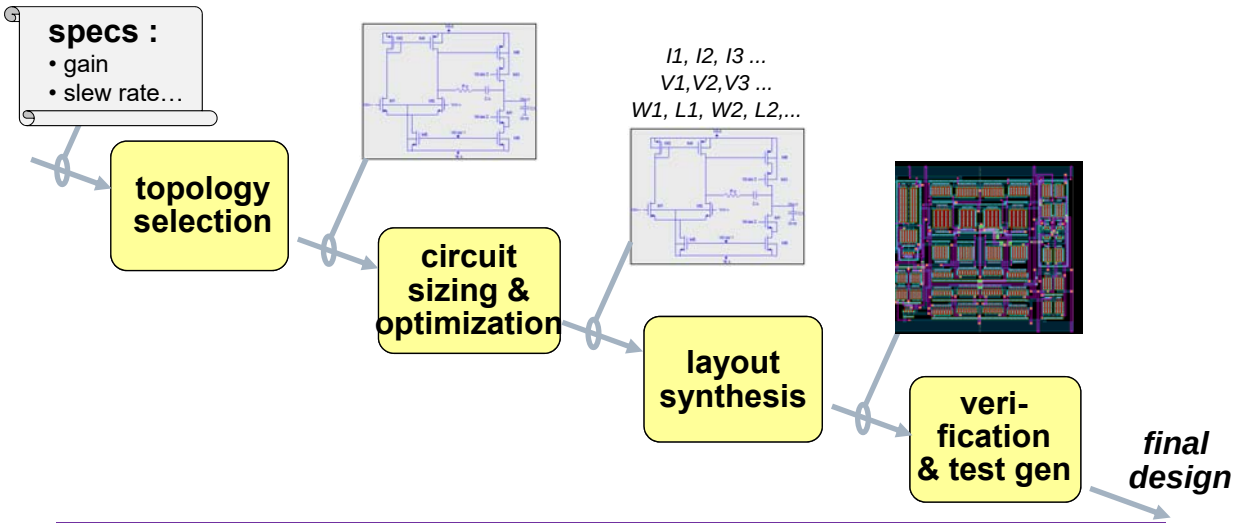
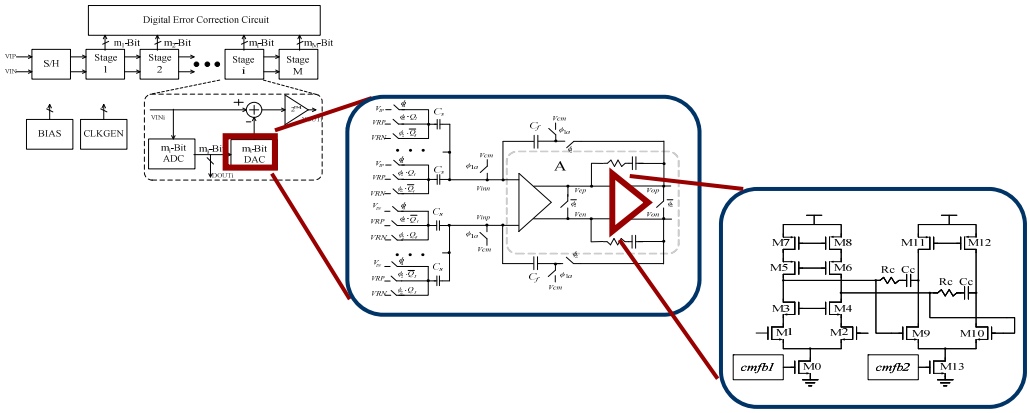
Typical analog design flow



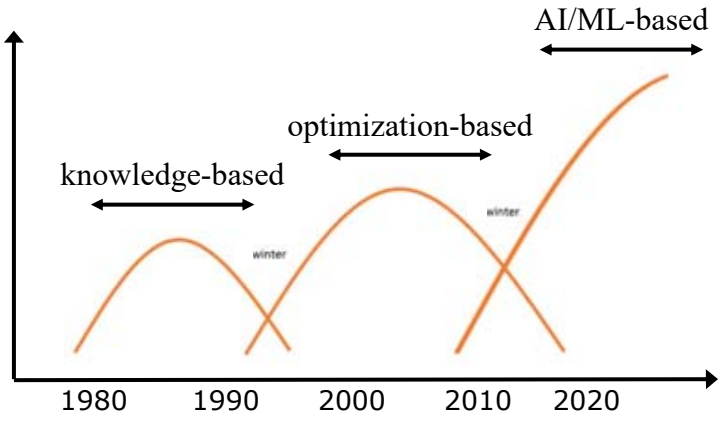
Analog design flow (2)

- flow repeated hierarchically for more complex blocks
  - behavioral at higher levels, moving towards transistor level at the bottom



Three waves of analog synthesis

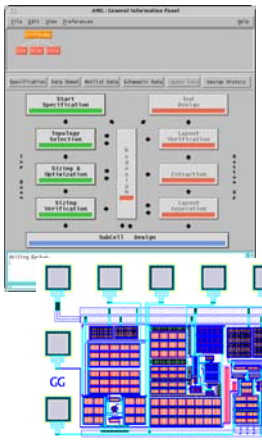
- three different technological approaches



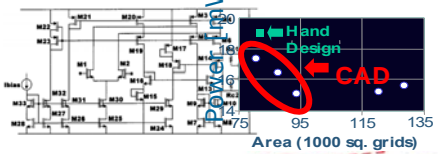
[Gielen & Rutenbar Proceedings IEEE 2000]

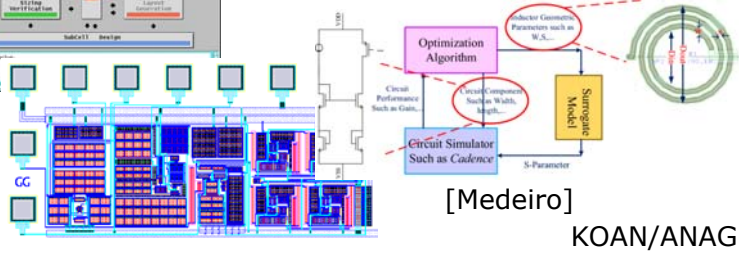
Some famous example tools

AMGIE [Van der Plas - IEEE TCAD 2001]



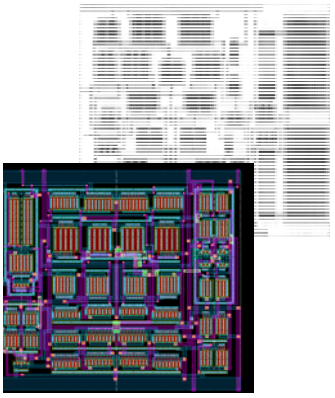
ANACONDA [Phelps - IEEE TCAD 2000]





[Medeiro]

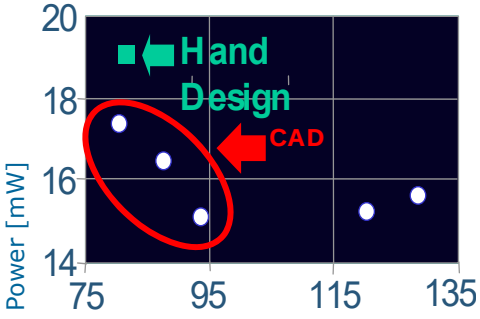
LAYLA [Lampaert - Springer 1999]



KOAN/ANAGRAM 2 [Cohn - IEEE JSSC 1991]

Weakness: long CPU times + need for constraints

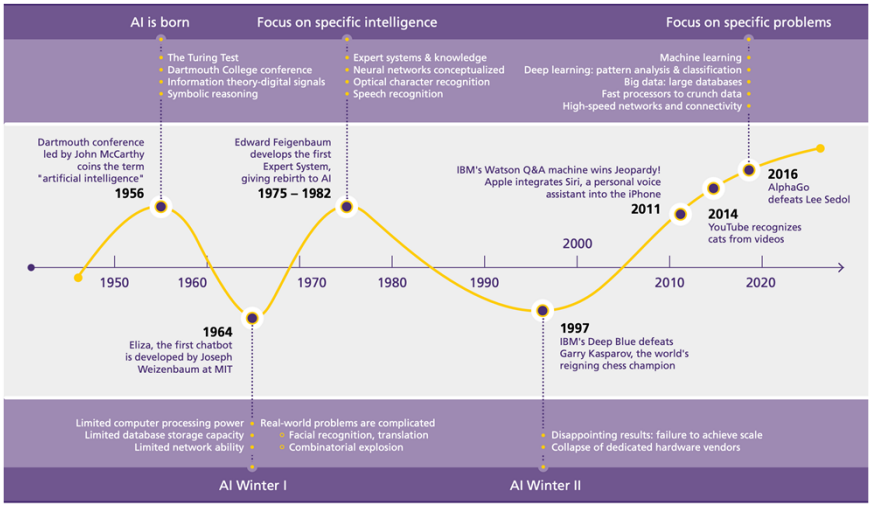
- analog CAD tools beat human designers!!



ANACONDA
[Phelps - TCAD 2000]

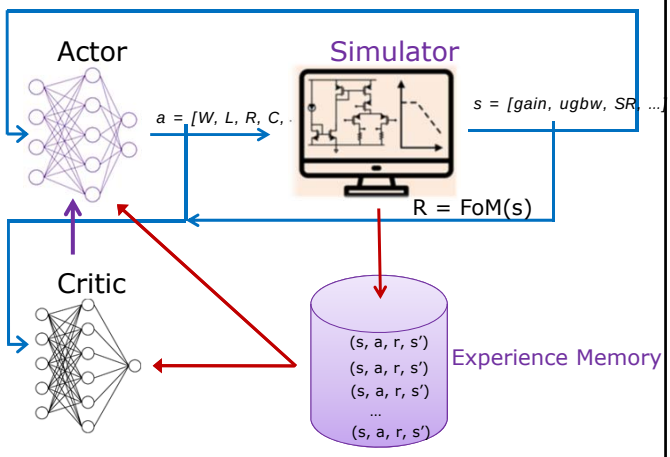
- but optimizers only give you exactly what you asked for

The rise of AI



Reinforcement learning with TD3

- actor & critic networks
- the actor network suggests sizes for the circuit
- a simulation is done for these sizes
- the critic network estimates expected value of future rewards
- the actor and critic networks are updated with past experiences at each step



[Ahmadzadeh & Gielen DAC 2024]

Reinforcement learning for analog circuit sizing

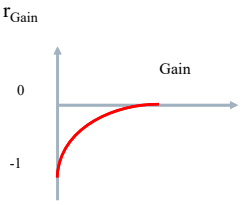
- state space:
  - list of current normalized performances
- action space:
  - W, L, R, C, …
- Figure of Merit (Reward):

$$z_y = \frac{y - y^*}{y + y^*} \rightarrow r_y = \begin{cases} \min(z_y, 0), & y \in Y_L \\ -\max(z_y, 0), & y \in Y_U \end{cases} \rightarrow r_H = \sum_{y \in Y} r_y$$

$$o_t = \frac{t - t^*}{t + t^*} \rightarrow r_t = o_t \rightarrow r_T = \sum_{t \in T} r_t$$

$$FoM = \begin{cases} r_H - \alpha \times r_T, & \text{if } r_H < 0 \\ 0.3 - \beta \times r_T, & \text{if } r_H = 0 \end{cases}$$

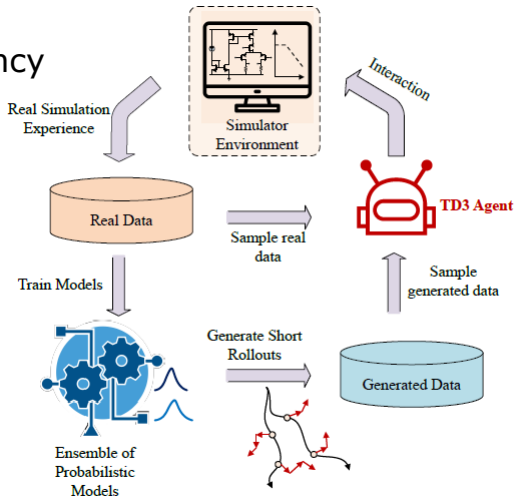
Reward = R =



Reinforcement learning with model rollouts

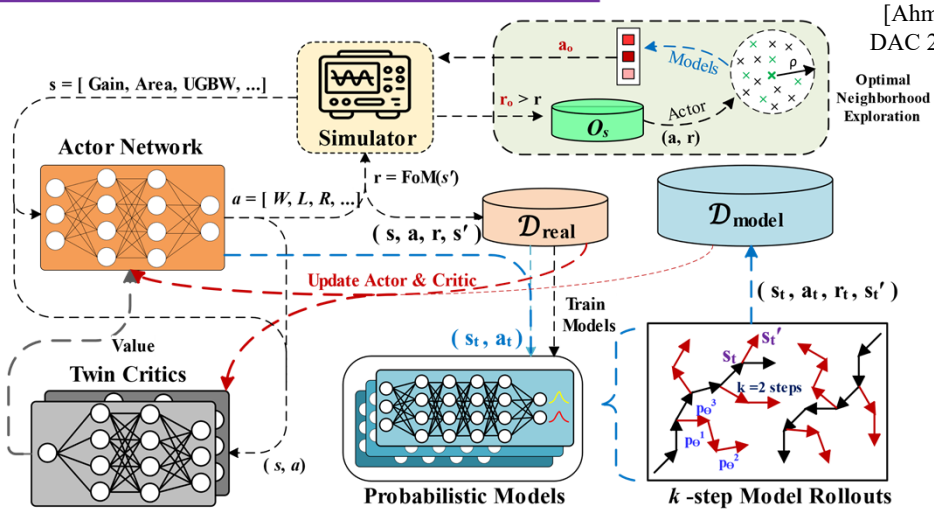
- apply Model-Based Policy Optimization (MBPO) to boost the RL sample efficiency
  - leverages an ensemble of probabilistic dynamic models to generate short rollouts branched from real data for a fast exploration of the design space
  - speeds up the learning process of the RL learning agent and improves its convergence
- efficiency gain:
  - up to ~3x fewer simulations and half the run time compared to model-free RL

[Ahmadzadeh & Gielen DAC 2024]

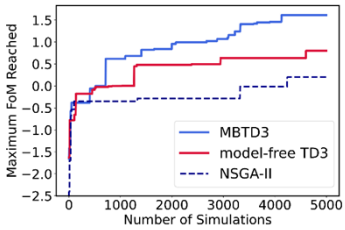


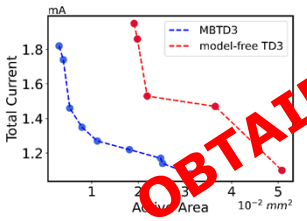
Full MBTD3 architecture for circuit sizing

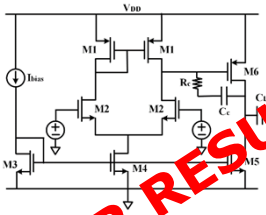
[Ahmadzadeh & Gielen DAC 2024 & TCAD 2025]

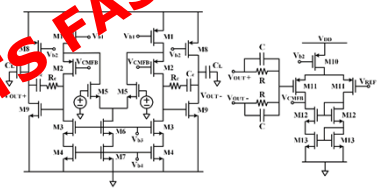


Example: operational amplifiers









OBTAINS BETTER RESULTS FASTER

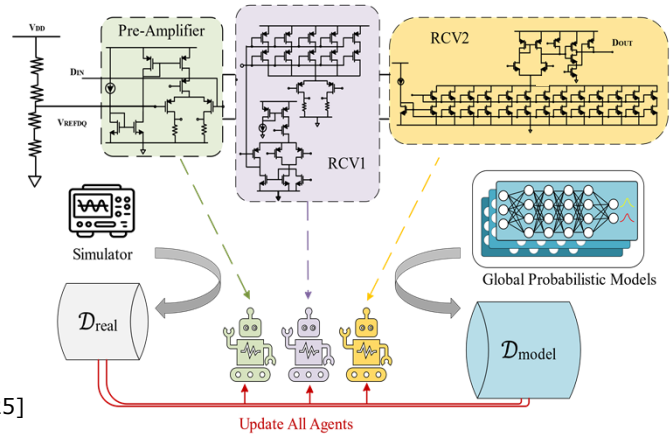
Comparison with model-free TD3

[Ahmadzadeh & Gielen DAC 2024 & TCAD 2025]

Performance	two-stage opamp			folded-cascode opamp		
	target	TD3	MBTD3	Target	TD3	MBTD3
Gain	200	221	237	350	417	455
Phase Margin (°)	60	78	75	60	64	67
Unity GBW (*MHz*)	1	19	24	10	178	186
Slew Rate ($V/\mu sec$)	15	28	26	15	18.2	24.2
Settling Time (μsec)	3	2.45	1.86	2	1.79	1.27
Out. Noise (mV_{rms})	10	7.4	5.6	30	26.7	23.6
Total Current (*mA*)	-	0.107	0.103	-	1.52	1.48
Area ($\times 10^{-3} mm^2$)	-	1.081	1.01	-	22.15	21.56
FoM	-	0.78	**0.9**	-	0.79	**0.81**
# Simulations	-	2926	**1452**	-	4283	**1417**
Runtime (*hours*)	-	2.24	**1.65**	-	3.57	**1.74**

Multi-agent version for more complex circuits

- multi-agent RL (MARL) variant for complex circuits
- using global models for predicting the output of all sub-blocks

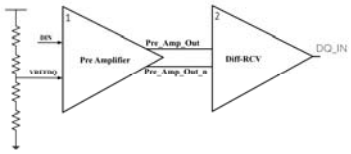


[Ahmadzadeh & Gielen DAC 2024]
[Ahmadzadeh & Gielen TCAD 2025]

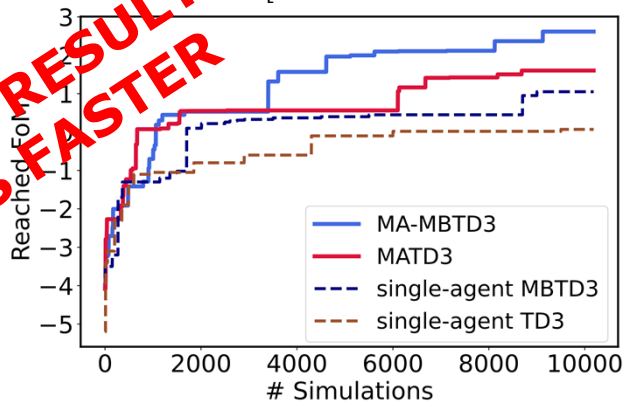
Example: data receiver circuit

- multi-agent version to deal with more complex circuits

[Ahmadzadeh & Gielen DAC 2024]
[Ahmadzadeh & Gielen TCAD 2025]



Performance	Target	MATD3	MA-MBTD3
Frequency (*GHz*)	> 2.33	2.19	2.487
Differential Slew Rate (*V/nsec*)	> 6		7.3
RCV2 Gain	-	75	9
Total Current (*mA*)	-	6.8	4
Area ($\times 10^{-3} mm^2$)	-	3	2.3
FoM	-	1.52	**1.94**
#Simulations	-	8620	**4598**
Runtime (hours)	-	14.33	**7.9**

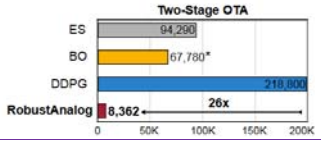


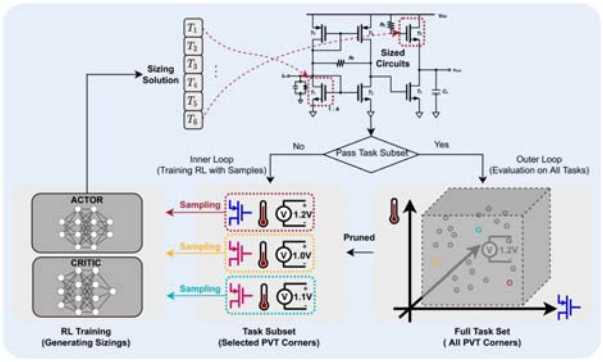
OBTAINS BETTER RESULTS THAN HUMANS FASTER

PVT-robustness ? Example: RobustAnalog

[Shi & al. MLCAD 2022]

- fast PVT variation-aware analog circuit design
  - via multi-task reinforcement learning
  - uses DDPG algorithm with actor & critic
  - prunes task subset (selected PVT corners)
  - reaches optimized and robust design result more efficiently





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- **ML-based analog layout synthesis**
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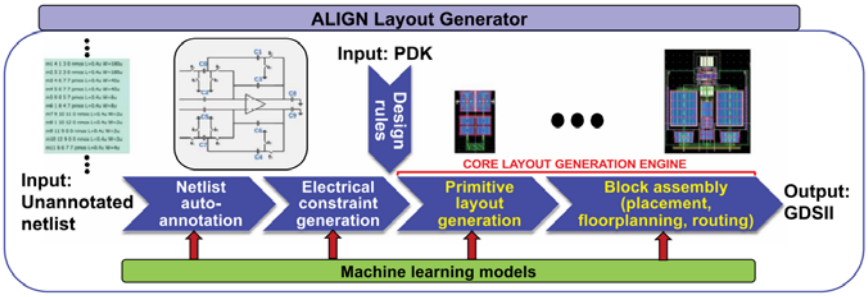
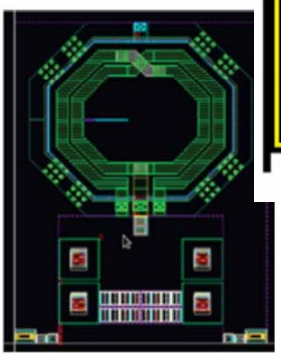
Example layout synthesis: ALIGN

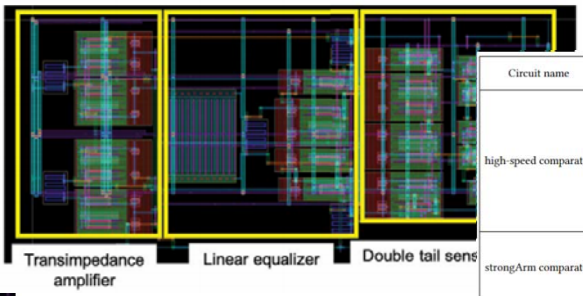
[Dhar IEEE Design & Test 2021]
[Dhar ASPDAC 2021]

- turns sized netlist into layout
  - uses hierarchical decomposition towards layout primitives
  - respects geometric and electric constraints
  - combines algorithmic/template-driven techniques with machine learning models
    - e.g. fast feasibility predictor for placements using SVM or MLP models



Example: ALIGN-generated layouts



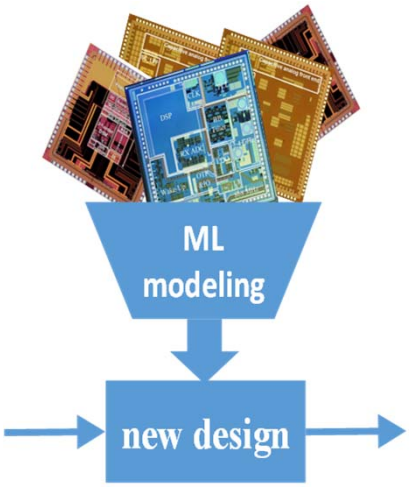


Circuit name	w/o. annotation and constraints	with functional group annotation	with transferred constraints
high-speed comparator			
strongArm comparator			
current-starved VCO			
clocked comparator			
cascode dynamic comparator			

[Dhar IEEE Design & Test 2021]

Extract constraints: AnalogCreate

- self-learn design constraints from many existing industrial designs
  - no human in the loop
  - reuse mostly at subblock level
- transfer learning to :
  - different designs of the same circuits
  - other circuits



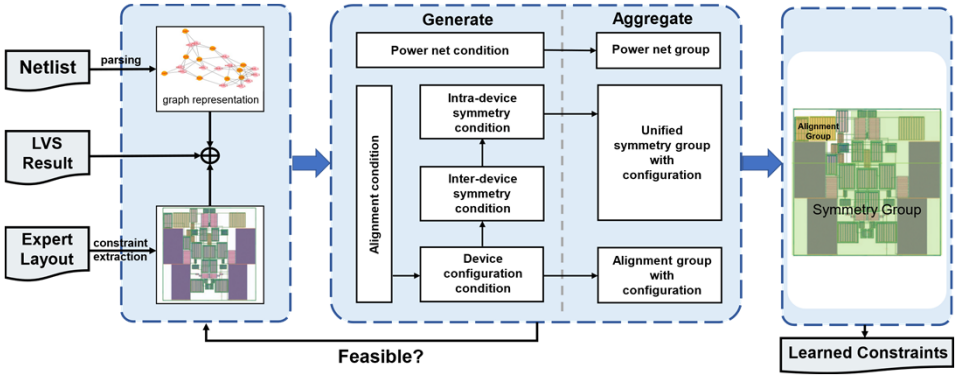
[Gielen ERC AnalogCreate]

Constraint learning-and-transfer methodology

- constraint learning system

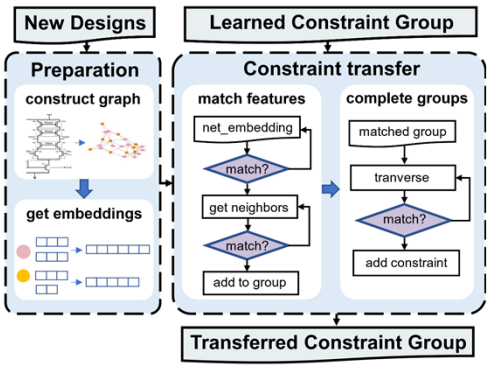
[Chen & Gielen DATE 2024 & TODAES 2025]

  - convert the expert design into a unified representation
  - learn constraints on the representation with generate-and-aggregate methodology



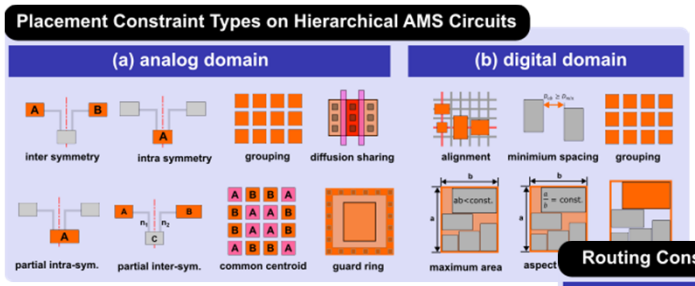
Constraint learning-and-transfer methodology

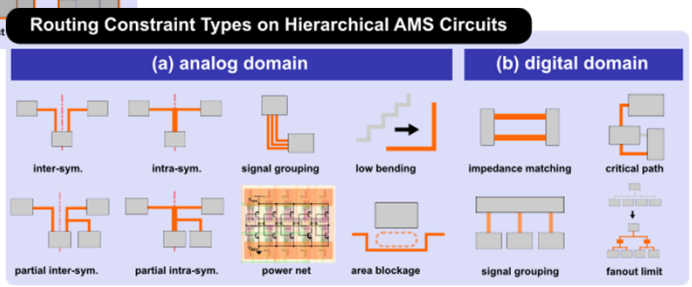
- constraint transfer system
  - represent new designs with bipartite graphs and add embeddings on each node
  - match node embeddings with those in the learned constraint group



[Chen & Gielen DATE 2024]
[Chen & Gielen TODAES 2025]

Placement and routing constraints

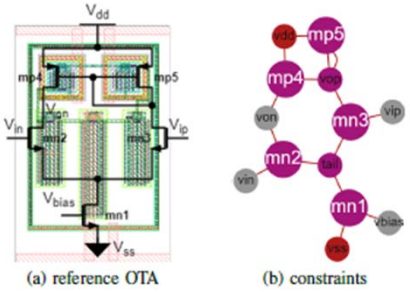




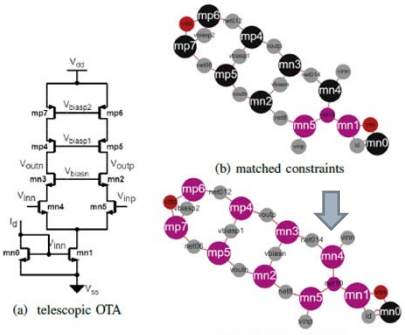
[Chen & Gielen TODAES 2025]

Learning and transfer examples

- partial matching on OTA [Chen & Gielen DATE 2024 & TODAES 2025]
  - learn symmetry constraints on an OTA
  - transfer and complete the symmetry constraints on a telescopic OTA



Constraint learning a five-transistor OTA.



Constraint transfer to a telescopic OTA.

Outline

- Analog/mixed-signal IC design
- ML-based analog circuit sizing
- ML-based analog layout synthesis
- **Conclusions**

Conclusions

- electronics are ubiquitous and enable the digital transformation in our society
  - analog/mixed-signal chips remain essential in a digital world
- CAD algorithms and tools are needed for the efficient/automated design of chips
  - use of AI/machine learning as effective algorithms
  - can handle complex circuits and PVT-robustness efficiently
  - can generate constraints for analog layout synthesis
  - early attempts to exploit generative AI are ongoing

Questions ?

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